**Second ALU:**

**Verilog Code:**

module secondaluu(

input [3:0] a,

input [3:0] b,

input cin1,

input [4:0] s,

output reg [3:0] Y

);

wire [3:0]Y1,Y2,Y3,Y4,Y5,Y6,Y7,Y8,Y9,Y10,Y11,Y12,Y13,Y14;

wire Carry4,Carry5,Carry6,Carry7;

trans trans1(a,Y1);

incre incre1(a,Y2,Carry4);

addition addition1(a,b,Y3,Carry5);

addcarry addcarry1(a,b,Y4,Carry6);

addcomple addcomple1(a,b,Y5,Carry7);

sub sub1(a,b,Y6);

decre decre1(a,Y7);

trans trans2(a,Y8);

andd andd1(a,b,Y9);

orr orr1(a,b,Y10);

exorr exorr1(a,b,Y11);

comple comple1(a,Y12);

shiftl shiftl1(a,Y13);

shiftr shiftr1(a,Y14);

always@(a,b,cin1,s,Y1,Y2,Y3,Y4,Y5,Y6,Y7,Y8,Y9,Y10,Y11,Y12,Y13,Y14)

begin

if(cin1==1'b0&&s==5'b00000)

Y=Y1;

else if(cin1==1'b1&&s==5'b00000)

Y=Y2;

else if(cin1==1'b0&&s==5'b00001)

Y=Y3;

else if(cin1==1'b1&&s==5'b00001)

Y=Y4;

else if(cin1==1'b0&&s==5'b00010)

Y=Y5;

else if(cin1==1'b1&&s==5'b00010)

Y=Y6;

else if(cin1==1'b0&&s==5'b00011)

Y=Y7;

else if(cin1==1'b1&&s==5'b00011)

Y=Y8;

else if(cin1==1'b0&&s==5'b00100)

Y=Y9;

else if(cin1==1'b0&&s==5'b00101)

Y=Y10;

else if(cin1==1'b0&&s==5'b00110)

Y=Y11;

else if(cin1==1'b0&&s==5'b00111)

Y=Y12;

else if(cin1==1'b0&&s==5'b01000)

Y=Y13;

else if(cin1==1'b0&&s==5'b10000)

Y=Y14;

else if (cin1==1'b0&&s==5'b11000)

Y=4'b0000;

else

Y=1'b0;

end

endmodule

**Testbench:**

module secondaluu\_tb;

// Inputs

reg [3:0] a;

reg [3:0] b;

reg cin1;

reg [4:0] s;

// Outputs

wire [3:0] Y;

// Instantiate the Unit Under Test (UUT)

secondaluu uut (

.a(a),

.b(b),

.cin1(cin1),

.s(s),

.Y(Y)

);

initial begin

// Initialize Inputs

a = 0;

b = 0;

cin1 = 0;

s = 0;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

a=4'b1111;

b=4'b1100;

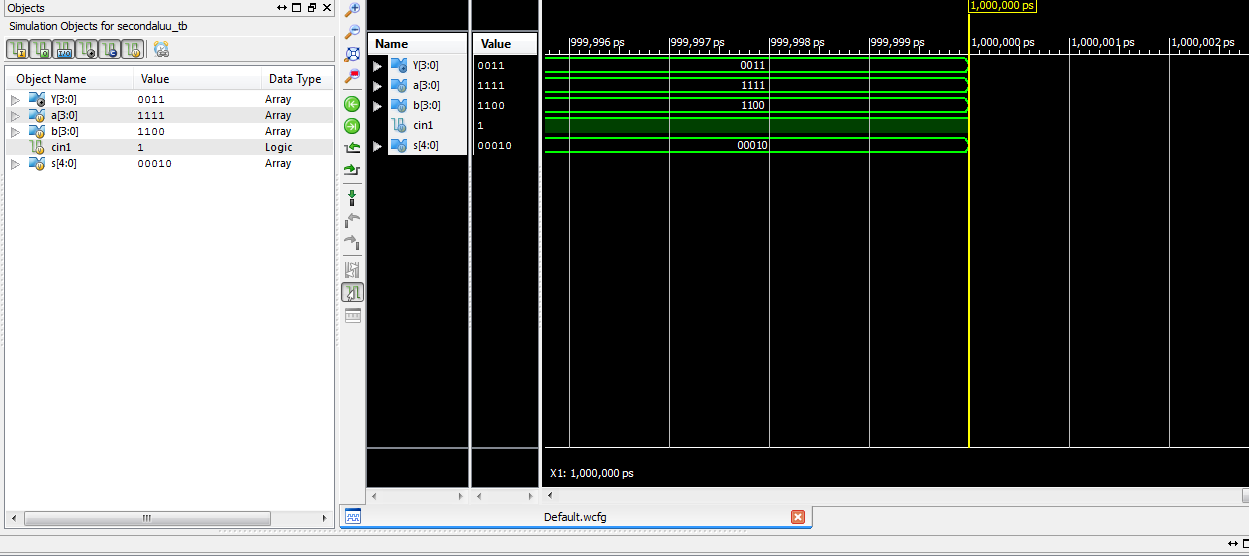
cin1=1'b1;

s=5'b00010;

#100;

end

endmodule



**Synthesis Report:**

Release 12.1 - xst M.53d (nt)

Copyright (c) 1995-2010 Xilinx, Inc. All rights reserved.

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.39 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.39 secs

--> Reading design: secondaluu.prj

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6.1) Advanced HDL Synthesis Report

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8) Partition Report

9) Final Report

9.1) Device utilization summary

9.2) Partition Resource Summary

9.3) TIMING REPORT

=========================================================================

\* Synthesis Options Summary \*

=========================================================================

---- Source Parameters

Input File Name : "secondaluu.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "secondaluu"

Output Format : NGC

Target Device : xc3s200-5-pq208

---- Source Options

Top Module Name : secondaluu

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : lut

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : YES

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : YES

Resource Sharing : YES

Asynchronous To Synchronous : NO

Multiplier Style : auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 8

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Yes

Use Synchronous Set : Yes

Use Synchronous Reset : Yes

Pack IO Registers into IOBs : auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Library Search Order : secondaluu.lso

Keep Hierarchy : NO

Netlist Hierarchy : as\_optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=========================================================================

=========================================================================

\* HDL Compilation \*

=========================================================================

Compiling verilog file "fulladder.v" in library work

Compiling verilog file "negone.v" in library work

Module <fulladder> compiled

Compiling verilog file "fulladderr.v" in library work

Module <negone> compiled

Compiling verilog file "fulladde.v" in library work

Module <fulladderr> compiled

Compiling verilog file "fulladd.v" in library work

Module <fulladde> compiled

Compiling verilog file "trans.v" in library work

Module <fulladd> compiled

Compiling verilog file "sub.v" in library work

Module <trans> compiled

Compiling verilog file "shiftr.v" in library work

Module <sub> compiled

Compiling verilog file "shiftl.v" in library work

Module <shiftr> compiled

Compiling verilog file "orr.v" in library work

Module <shiftl> compiled

Compiling verilog file "incre.v" in library work

Module <orr> compiled

Compiling verilog file "exorr.v" in library work

Module <incre> compiled

Compiling verilog file "decre.v" in library work

Module <exorr> compiled

Compiling verilog file "comple.v" in library work

Module <decre> compiled

Compiling verilog file "andd.v" in library work

Module <comple> compiled

Compiling verilog file "addition.v" in library work

Module <andd> compiled

Compiling verilog file "addcomple.v" in library work

Module <addition> compiled

Compiling verilog file "addcarry.v" in library work

Module <addcomple> compiled

Compiling verilog file "secondaluu.v" in library work

Module <addcarry> compiled

Module <secondaluu> compiled

No errors in compilation

Analysis of file <"secondaluu.prj"> succeeded.

=========================================================================

\* Design Hierarchy Analysis \*

=========================================================================

Analyzing hierarchy for module <secondaluu> in library <work>.

Analyzing hierarchy for module <trans> in library <work>.

Analyzing hierarchy for module <incre> in library <work>.

Analyzing hierarchy for module <addition> in library <work>.

Analyzing hierarchy for module <addcarry> in library <work>.

Analyzing hierarchy for module <addcomple> in library <work>.

Analyzing hierarchy for module <sub> in library <work>.

Analyzing hierarchy for module <decre> in library <work>.

Analyzing hierarchy for module <andd> in library <work>.

Analyzing hierarchy for module <orr> in library <work>.

Analyzing hierarchy for module <exorr> in library <work>.

Analyzing hierarchy for module <comple> in library <work>.

Analyzing hierarchy for module <shiftl> in library <work>.

Analyzing hierarchy for module <shiftr> in library <work>.

Analyzing hierarchy for module <fulladder> in library <work>.

Analyzing hierarchy for module <fulladderr> in library <work>.

Analyzing hierarchy for module <fulladd> in library <work>.

Analyzing hierarchy for module <fulladde> in library <work>.

Analyzing hierarchy for module <negone> in library <work>.

Analyzing hierarchy for module <fulladder> in library <work>.

Analyzing hierarchy for module <fulladder> in library <work>.

Analyzing hierarchy for module <fulladder> in library <work>.

Analyzing hierarchy for module <fulladder> in library <work>.

=========================================================================

\* HDL Analysis \*

=========================================================================

Analyzing top module <secondaluu>.

Module <secondaluu> is correct for synthesis.

Analyzing module <trans> in library <work>.

Module <trans> is correct for synthesis.

Analyzing module <incre> in library <work>.

Module <incre> is correct for synthesis.

Analyzing module <fulladder> in library <work>.

Module <fulladder> is correct for synthesis.

Analyzing module <addition> in library <work>.

Module <addition> is correct for synthesis.

Analyzing module <fulladderr> in library <work>.

Module <fulladderr> is correct for synthesis.

Analyzing module <addcarry> in library <work>.

Module <addcarry> is correct for synthesis.

Analyzing module <fulladd> in library <work>.

Module <fulladd> is correct for synthesis.

Analyzing module <addcomple> in library <work>.

Module <addcomple> is correct for synthesis.

Analyzing module <fulladde> in library <work>.

Module <fulladde> is correct for synthesis.

Analyzing module <sub> in library <work>.

Module <sub> is correct for synthesis.

Analyzing module <negone> in library <work>.

Module <negone> is correct for synthesis.

Analyzing module <decre> in library <work>.

Module <decre> is correct for synthesis.

Analyzing module <andd> in library <work>.

Module <andd> is correct for synthesis.

Analyzing module <orr> in library <work>.

Module <orr> is correct for synthesis.

Analyzing module <exorr> in library <work>.

Module <exorr> is correct for synthesis.

Analyzing module <comple> in library <work>.

Module <comple> is correct for synthesis.

Analyzing module <shiftl> in library <work>.

Module <shiftl> is correct for synthesis.

Analyzing module <shiftr> in library <work>.

Module <shiftr> is correct for synthesis.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <trans>.

Related source file is "trans.v".

Unit <trans> synthesized.

Synthesizing Unit <andd>.

Related source file is "andd.v".

Unit <andd> synthesized.

Synthesizing Unit <orr>.

Related source file is "orr.v".

Unit <orr> synthesized.

Synthesizing Unit <exorr>.

Related source file is "exorr.v".

Found 4-bit xor2 for signal <Y>.

Unit <exorr> synthesized.

Synthesizing Unit <comple>.

Related source file is "comple.v".

Unit <comple> synthesized.

Synthesizing Unit <shiftl>.

Related source file is "shiftl.v".

[WARNING](WARNING:Xst:647%20-%20Input%20%3ca%3c3%3e%3e%20is%20never%20used.%20This%20port%20will%20be%20preserved%20and%20left%20unconnected%20if%20it%20belongs%20to%20a%20top-level%20block%20or%20it%20belongs%20to%20a%20sub-block%20and%20the%20hierarchy%20of%20this%20sub-block%20is%20preserved.?&DataKey=SolutionRecord):Xst:647 - Input <a<3>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

Unit <shiftl> synthesized.

Synthesizing Unit <shiftr>.

Related source file is "shiftr.v".

[WARNING](WARNING:Xst:647%20-%20Input%20%3ca%3c0%3e%3e%20is%20never%20used.%20This%20port%20will%20be%20preserved%20and%20left%20unconnected%20if%20it%20belongs%20to%20a%20top-level%20block%20or%20it%20belongs%20to%20a%20sub-block%20and%20the%20hierarchy%20of%20this%20sub-block%20is%20preserved.?&DataKey=SolutionRecord):Xst:647 - Input <a<0>> is never used. This port will be preserved and left unconnected if it belongs to a top-level block or it belongs to a sub-block and the hierarchy of this sub-block is preserved.

Unit <shiftr> synthesized.

Synthesizing Unit <fulladder>.

Related source file is "fulladder.v".

Found 1-bit xor3 for signal <Sum>.

Summary:

inferred 1 Xor(s).

Unit <fulladder> synthesized.

Synthesizing Unit <fulladderr>.

Related source file is "fulladderr.v".

Found 1-bit xor3 for signal <Sum>.

Summary:

inferred 1 Xor(s).

Unit <fulladderr> synthesized.

Synthesizing Unit <fulladd>.

Related source file is "fulladd.v".

Found 1-bit xor3 for signal <Sum>.

Summary:

inferred 1 Xor(s).

Unit <fulladd> synthesized.

Synthesizing Unit <fulladde>.

Related source file is "fulladde.v".

Found 1-bit xor3 for signal <Sum>.

Summary:

inferred 1 Xor(s).

Unit <fulladde> synthesized.

Synthesizing Unit <incre>.

Related source file is "incre.v".

Unit <incre> synthesized.

Synthesizing Unit <addition>.

Related source file is "addition.v".

Unit <addition> synthesized.

Synthesizing Unit <addcarry>.

Related source file is "addcarry.v".

Unit <addcarry> synthesized.

Synthesizing Unit <addcomple>.

Related source file is "addcomple.v".

Unit <addcomple> synthesized.

Synthesizing Unit <negone>.

Related source file is "negone.v".

Unit <negone> synthesized.

Synthesizing Unit <sub>.

Related source file is "sub.v".

[WARNING](WARNING:Xst:646%20-%20Signal%20%3cCarry5%3e%20is%20assigned%20but%20never%20used.%20This%20unconnected%20signal%20will%20be%20trimmed%20during%20the%20optimization%20process.?&DataKey=SolutionRecord):Xst:646 - Signal <Carry5> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Unit <sub> synthesized.

Synthesizing Unit <decre>.

Related source file is "decre.v".

[WARNING](WARNING:Xst:646%20-%20Signal%20%3cCarry5%3e%20is%20assigned%20but%20never%20used.%20This%20unconnected%20signal%20will%20be%20trimmed%20during%20the%20optimization%20process.?&DataKey=SolutionRecord):Xst:646 - Signal <Carry5> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Unit <decre> synthesized.

Synthesizing Unit <secondaluu>.

Related source file is "secondaluu.v".

[WARNING](WARNING:Xst:646%20-%20Signal%20%3cCarry7%3e%20is%20assigned%20but%20never%20used.%20This%20unconnected%20signal%20will%20be%20trimmed%20during%20the%20optimization%20process.?&DataKey=SolutionRecord):Xst:646 - Signal <Carry7> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

[WARNING](WARNING:Xst:646%20-%20Signal%20%3cCarry6%3e%20is%20assigned%20but%20never%20used.%20This%20unconnected%20signal%20will%20be%20trimmed%20during%20the%20optimization%20process.?&DataKey=SolutionRecord):Xst:646 - Signal <Carry6> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

[WARNING](WARNING:Xst:646%20-%20Signal%20%3cCarry5%3e%20is%20assigned%20but%20never%20used.%20This%20unconnected%20signal%20will%20be%20trimmed%20during%20the%20optimization%20process.?&DataKey=SolutionRecord):Xst:646 - Signal <Carry5> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

[WARNING](WARNING:Xst:646%20-%20Signal%20%3cCarry4%3e%20is%20assigned%20but%20never%20used.%20This%20unconnected%20signal%20will%20be%20trimmed%20during%20the%20optimization%20process.?&DataKey=SolutionRecord):Xst:646 - Signal <Carry4> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

Unit <secondaluu> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Xors : 33

1-bit xor3 : 32

4-bit xor2 : 1

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Xors : 33

1-bit xor3 : 32

4-bit xor2 : 1

=========================================================================

=========================================================================

\* Low Level Synthesis \*

=========================================================================

[WARNING](WARNING:Xst:1989%20-%20Unit%20%3csecondaluu%3e:%20instances%20%3ctrans1%3e,%20%3ctrans2%3e%20of%20unit%20%3ctrans%3e%20are%20equivalent,%20second%20instance%20is%20removed?&DataKey=SolutionRecord):Xst:1989 - Unit <secondaluu>: instances <trans1>, <trans2> of unit <trans> are equivalent, second instance is removed

Optimizing unit <secondaluu> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block secondaluu, actual ratio is 2.

Final Macro Processing ...

=========================================================================

Final Register Report

Found no macro

=========================================================================

=========================================================================

\* Partition Report \*

=========================================================================

Partition Implementation Status

-------------------------------

No Partitions were found in this design.

-------------------------------

=========================================================================

\* Final Report \*

=========================================================================

Final Results

RTL Top Level Output File Name : secondaluu.ngr

Top Level Output File Name : secondaluu

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : NO

Design Statistics

# IOs : 18

Cell Usage :

# BELS : 85

# GND : 1

# LUT2 : 3

# LUT3 : 17

# LUT4 : 58

# MUXF5 : 6

# IO Buffers : 18

# IBUF : 14

# OBUF : 4

=========================================================================

Device utilization summary:

---------------------------

Selected Device : 3s200pq208-5

Number of Slices: 45 out of 1920 2%

Number of 4 input LUTs: 78 out of 3840 2%

Number of IOs: 18

Number of bonded IOBs: 18 out of 141 12%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

---------------------------

=========================================================================

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

No clock signals found in this design

Asynchronous Control Signals Information:

----------------------------------------

No asynchronous control signals found in this design

Timing Summary:

---------------

Speed Grade: -5

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 15.055ns

Timing Detail:

--------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default path analysis

Total number of paths / destination ports: 410 / 4

-------------------------------------------------------------------------

Delay: 15.055ns (Levels of Logic = 8)

Source: cin1 (PAD)

Destination: Y<3> (PAD)

Data Path: cin1 to Y<3>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 13 0.715 1.290 cin1\_IBUF (cin1\_IBUF)

LUT4:I0->O 8 0.479 1.216 Y\_and000811 (N3)

LUT3:I0->O 2 0.479 0.915 Y\_and00091 (Y\_and0009)

LUT4:I1->O 1 0.479 0.740 Y<3>4 (Y<3>4)

LUT4:I2->O 1 0.479 0.976 Y<3>105 (Y<3>105)

LUT3:I0->O 1 0.479 0.740 Y<3>173 (Y<3>173)

LUT4:I2->O 1 0.479 0.681 Y<3>299 (Y\_3\_OBUF)

OBUF:I->O 4.909 Y\_3\_OBUF (Y<3>)

----------------------------------------

Total 15.055ns (8.498ns logic, 6.557ns route)

(56.4% logic, 43.6% route)

=========================================================================

Total REAL time to Xst completion: 11.00 secs

Total CPU time to Xst completion: 11.29 secs

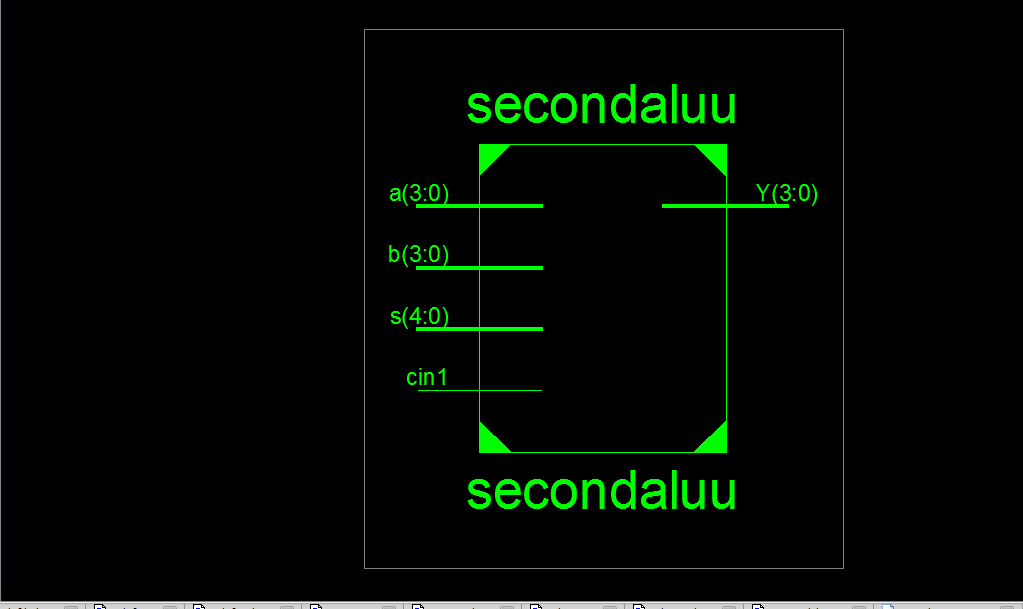
-->

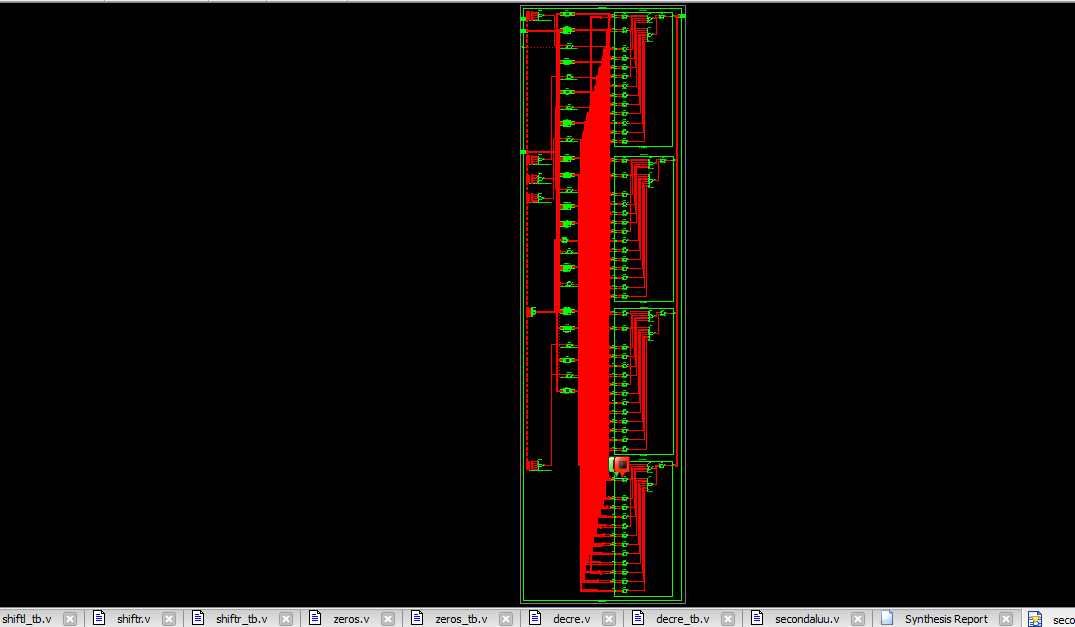
Total memory usage is 189304 kilobytes

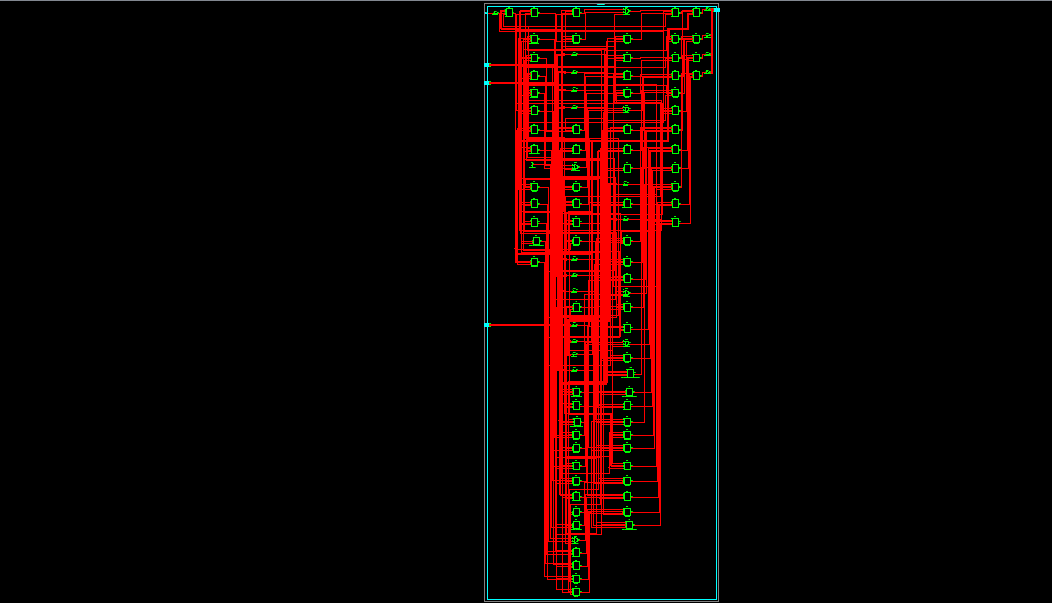
Number of errors : 0 ( 0 filtered)

Number of warnings : 9 ( 0 filtered)

Number of infos : 0 ( 0 filtered)

****

****

****